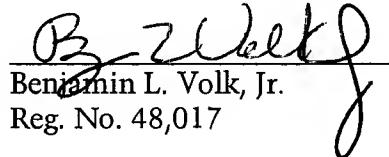


**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**  
**CERTIFICATE OF E-FILING**

I hereby certify that this correspondence has been e-filed with the U.S. Patent and Trademark Office on March 10, 2010.

  
Benjamin L. Volk, Jr.  
Reg. No. 48,017

In re application of: Chamberlain et al.	:	
Serial No.: 10/550,326	:	Examiner: Roderick Tolentino
Filed: January 9, 2007	:	Group Art Unit: 2439
For: Intelligent Data Storage and Processing	:	
Using FPGA Devices	:	

Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

**ELECTION IN RESPONSE TO RESTRICTION**  
**REQUIREMENT DATED FEBRUARY 3, 2010**

In response to the Restriction Requirement dated February 3, 2010, Applicant files the following election.

Claims are reflected in the listing of claims which begins on page 2 of this paper.

Remarks begin on page 6 of this paper.